IN THE CLAIMS

1. (Currently Amended) A processor, comprising:

a plurality of registers;

circuitry configured to process a plurality of instructions associated with an instruction set including a plurality of branch and non-branch instructions, the plurality of instructions each having a multi-byte length, the plurality of instructions accessible at multi-byte aligned addresses;

common subcircuitry operable to perform sign extensions of an immediate field in non-branch instructions and to perform sign extensions of said immediate field in branch instructions to calculate a target address for branch instructions**, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions**; and

wherein substantially all multi-byte aligned branch instructions are operable to access the instructions at byte aligned addresses.

2. (Original) The processor of claim 1, wherein the plurality of instructions are accessed at word aligned addresses.

3. (Original) The processor of claim 1, wherein the plurality of instructions are accessed at half-word aligned addresses.

4. (Original) The processor of claim 1, wherein accessing the instructions comprises reading and writing the addresses.